Amendments to the Specification:

Please replace the paragraph beginning on page 2, line 21, with the following amended paragraph:

An alternative or adjunct to functional testing is "structural" testing. Structural testing became of interest in the mid-1970's, and is discussed in detail in the paper of M.J.Y. Williams and J.B. ~~Angel~~Angell entitled "~~Enhanced~~Enhancing Testability of ~~Large Scale~~Large-Scale Integrated Circuits Via Test Points and Additional Logic", *IEEE Trans. on Computers*, vol. C-22, no. 1, pp. 46-60 (Jan. 1973), and in the paper of E.B. ~~Eicherberger~~Eichelberger and T.W. Williams entitled "A Logic Design Structure for LSI ~~Testing~~Testability", *Proc. 14th Design Automation Conf.*, IEEE Pub. 77CH1216-1C, pp. 462-468 (June 1977), which papers are hereby incorporated by reference for all that they disclose. Initially called "scan" testing, structural testing enables the testing of structures which are deeply embedded within an IC. Rather than testing the IC's internal structure by applying stimulus to the IC's inputs, structural testing involves shifting a series of test vectors into the core of an IC, and after each test vector is shifted in, launching the test vector and capturing a response. Each response is then shifted out of the IC. In this manner, a tester can verify that all of an IC's elements are present and operational. An assumption of structural testing is that if all elements are present and operational, then the elements will contribute to performing the greater and intended functions of an IC (e.g., adding, shifting, etc.), and the IC will function as designed.

Please replace the paragraph beginning on page 3, line 30, with the following amended paragraph:

If desired, structural testing can be expanded to the board level. When designing a board, a designer can link signals of each IC at the board level (e.g., mode, shift and data I/O signals) to thereby expand structural testing to the board test level. A detailed discussion of various scan chains may be found in the paper of T.W.

Williams and K.P. Parker entitled "Design for Testability - A Survey", *Proceedings of the IEEE*, (Invited paper), vol. 71, no. 1, pp. 98-112 (Jan. 1983).